SMIC MPW Shuttle Schedule

MPW Notice To serve all customers smoothly, following items must be noticed:

1. Only standard Process/Layers products can attend MPW. No bumping, No Bank and No Corner Split allowed.
2. On one shuttle, 4 seats (including sub-chip in one seat) are the maximum that one customer can get.
3. **MPW only provides 50 dies for function verification.**
4. Shuttles are subject to cancellation if there are not enough passengers on board.
5. Without completion of below items before shuttle start date, shuttle reservation will not be held!

*Quotation should be ready/ DRC must be clean/ SMIC IP merge case must be closed (related information need to be submitted at least 3 days before shuttle start date)
*GDSII and tape out forms all need to be Approved by mask shop/ PTOS should be Approved

6. SMIC dicing size limit: 1500um < X < 12000um, 1500um < Y < 12000um.
7. For 300mm shuttle, suggest use metal scheme condition: 6(M1-M6)+TM1(9kA)+TM2(9kA)+14.5kA ALPA+12mil BG.
8. Overdue MPW booked cases will be cancelled within 90 days after shuttle start.

Tech Node	IO Voltage/Tech Type/Char	RF	2020 MPW Booking Cut-Off Date											
			Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
14nm	IO=1.8V **CMOS Logic (GE|GP)**				10 Q67 (Fab8)			9 Q6P (Fab8)			8 Q6Z (Fab8)			8 Q7C (Fab8)
28nm	IO=1.8V | IO=2.5V **CMOS Logic (HP)**	Y			3 Q6D (Fab2)			2 Q6Q (Fab2)			1 Q6Y (Fab2)			
40nm	IO=2.5V **CMOS Logic (LL|UP)**	Y		4 Q69 (Fab2)			5 Q6K (Fab2)		7 Q6T (Fab2)			13 Q73 (Fab2)		1 Q79 (Fab2)
	IO=8/32V **CMOS High Voltage (HV)**													
	IO=1.8V| IO=2.5V **Adv. Emb-Flash (Cu-BEOL with AL-TM2 + RDL process) (LL)**							23 Q6R (Fab2)						15 Q7B (Fab2)
55nm	IO=2.5/5V | IO=2.5V **Adv. Emb-Flash (Cu-BEOL) (LL)**						12 Q6M (Fab2)						10 Q77 (Fab2)	
	IO=1.8/2.5V | IO=1.8V| IO=2.5V **CMOS Logic (LL)**	Y		11 Q6C (Fab2)		7 Q6G (Fab2)			14 Q6U (Fab2)			20 Q74 (Fab2)		
	IO=6/32V | IO=8/32V **CMOS High Voltage (HV)** **Do not support 2XTM(STM)**													
0.11um	IO=3.3V **Adv. Emb-Super flash (AL-BEOL) (LL)**										8 Q70 (Fab1)			
0.13um	IO=3.3/5V| IO=5V **Adv. Emb-EEPROM (Cu-BEOL) (LL)**									4 Q6V (Fab1)				
0.11/0.13um	IO=3.3V **CMOS Logic (GE)|Mixed Signal (GE)**	Y		4 Q6B (Fab1)		14 Q6H (Fab1)		30 Q6S (Fab1)		11 Q6W (Fab1)		27 Q75 (Fab1)		29 Q7D (Fab1)
0.153um	IO=3.3V **CMOS Logic (GE)|Mixed Signal (GE)**	Y								18 Q6X (Fab1)				
0.18um	IO=5/6/9/12/16/20/24/30/35/40 **BCD V3E (EP)**				3 Q6E (Fab1)						15 Q71 (Fab7)			
	IO=3.3V **CMOS Logic (GE)|Mixed Signal (GE)**	Y	1 Q68 (Fab1)				19 Q6N (Fab1)				15 Q72 (Fab1)			
0.18um	IO=3.3V **CMOS Logic (GE)|Mixed Signal (GE)** IO=5/10/12/20/35/40V **BCDM (BCDM do not support RF)**	Y			10 Q6F (Fab7)				21 Q6J (Fab7)				17 Q78 (Fab7)	
	IO=3.3/5V| IO=5V **EEPROM Embedded (GE)**					14 Q6L (Fab1)						27 Q76 (Fab7)		

* 2020 new offered feature: 40nm EF/0.11um EF

Version: 1.1 Update Date: 2019-10-15

Note: Please login SMIC-Now to find the most updated MPW schedule. (请登录Smic-Now以查阅最新MPW Schedule.)